

REMARKS

Claims 1-3, 5, 7, 8, 11, 12, 14, 19, 20, 24, 30 and 32-34 are pending. By this Amendment, claims 1, 2, 7, 11, 14, 19, 24, 30, 32 and 34 are amended.

The Office Action states a formality objection to specification page 3, line 15. However, the objection is not understood; the cited text appears to be clear. Also, what the Examiner suggests as a correction appears to be no different than the quoted present language. Should the objection be maintained, clarification thereof is respectfully requested.

Claims 1-3, 5, 7-8 and 30 were rejected under 35 U.S.C. §112, second paragraph. The Examiner questions whether the recitation “emulation state circuit elements” in these claims is intended to be different from “emulation circuit elements” used in claim 11. No difference is intended. For added clarity and consistency, each of claims 1, 2, 7, 11, 30, 32 and 34 are amended to refer to “emulated circuit elements.” Accordingly, reconsideration and withdrawal of the rejections are respectfully requested.

All of the pending claims stand rejected under 35 U.S.C. §103(a) as being unpatentable over Quayle et al. U.S. Patent No. 6,694,464 in view of the deVries et al. article “Built-in Self Test Methodology for A/D Converters”. This rejection is respectfully traversed, particularly in light of the clarifying amendments presented herein.

As the Office Action acknowledges, the Quayle et al. patent does not disclose on-chip data processing resources used in the local generation and application of testing stimuli. Rather, Quayle et al. describe that code providing a behavioral test bench may be executed “in parallel on processors 206 of one or more of logic boards 200.” Column 31, lines 64-67.

For the feature of on-chip testing, the Office Action cites the deVries et al. article, and it is asserted that it would have been obvious to one of ordinary skill in the art “to modify the logic

board of Quayle et al. with the logic board of Vries et al. [sic] that included at least one of the emulation ICs comprising on-chip data processing resources to cooperate and assist the on-board data processing resources to perform the local generation and application of testing stimuli.”

This assertion is specifically traversed.

The deVries et al. article teaches a “built-in self-test methodology” for testing a fabricated (physical) integrated circuit (an A/D converter IC) to identify faulty devices, not data processing resources that locally generate and apply testing stimuli to emulation circuit elements (reconfigurable logic). deVries et al. physical device testing is very different from the testing of reconfigurable logic mapped to reconfigurable logic chips. In contrast to deVries physical device testing, the test bench testing of Quayle et al. is a testing of reconfigurable logic, i.e., testing to see whether the behavior of specified logic, mapped to logic chips, meets the intended objectives; this testing occurs before any fabrication of a physical IC. Thus, one of ordinary skill in the art would **not** have found deVries et al.’s built-in self-test (BIST) methodology to have applicability to the logical testing of Quayle et al., and would **not** have found it obvious to combine the references as proposed.

Moreover, even if one were to make the asserted combination of Quayle et al. and deVries et al., the claimed inventions would not result. As set forth in the clarified claims presented herewith, the on-chip data processing resources of the inventions are on-chip programmable data processing resources. For example, the specification, page 20, lines 5-8, describes that the on-chip data processing resources 1002 illustrated in Fig. 10 may execute selected ones of the software components illustrated in Fig. 4 (which include Test Stimuli Generator/Applicator 410). On the other hand, the result of the asserted combination would be an integrated circuit with fixed-function built-in self-test (BIST) circuitry.

For all of the foregoing reasons, it is respectfully submitted that this application is in condition for allowance. Should the Examiner believe that anything further is desirable in order to place the application in even better form for allowance, he is respectfully urged to telephone applicant's undersigned representative at the below-listed number.

Respectfully submitted,

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